Fig. 21 is a flow diagram showing processing sequence of a CPU in an external controller; and

Fig. 22 is a characteristic diagram showing a temperature rise of a Zener diode in a conventional alternator.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The preferred embodiments of the present invention will be explained with reference to various embodiments and modifications shown in the accompanying drawings.

[First Embodiment]

An alternator 1 for a vehicle comprises a three-phase armature winding 3, a full-wave rectifier 4, a field winding 5 and a voltage regulator 6. The full-wave rectifier 4 charges an on-board battery 2 through a power supply line 8 by converting AC output of the armature winding 3 to a DC output. The field winding 5 is wound about a rotor including a plurality of field poles to generate an inter-linkage magnetic flux to induce voltage and forms a field by applying a field current. The voltage regulator 6 adjusts DC output voltage of the alternator 1 for a vehicle to a predetermined voltage Vreg.

The voltage regulator 6 comprises a power transistor 61 reflux or flywheel diode 62, a main power supply circuit 63, a filter 64, a first comparator 65, a second comparator 66, a timer circuit 67, an inverter 68, an AND gate 69, a pulse generator 70, and an OR gate 71. The second comparator 66 is for detecting a failure, while the timer circuit 67 and AND gate 69 are for controlling or suppressing power generation.

The power transistor 61 is a switch means connected in series to the field winding 5 for ON/OFF-control of the field current flowing into the field winding 5. The flywheel diode 62 is a flywheel circuit connected in parallel with the field winding 5 to flywheel the field current when the power transistor 61 is turned off (opened). The main power supply circuit 63 detects the turning-on condition of an on-board key switch 7 to form the drive power supply, Vcc of the voltage regulator 6 from the on-board battery 2. The filter 64 absorbs harmonics noise superimposed on an output voltage of the full-wave rectifier 4. The first comparator 65 compares the output voltage of the filter 64 with the predetermined value Vreg, and provides an inverted output when the output voltage of the alternator 1 is smaller than the predetermined value Vreg.

The second comparator 66 compares the output of the filter 64 with the predetermined value Vreg+$\alpha$, and provides an inverted output when the output voltage of the alternator 1 exceeds the predetermined value Vreg+$\alpha$. The timer circuit 67 inputs the output signal of the second comparator 66 and provides an inverted output only for the predetermined period from a rising edge of the output signal of the second comparator 66. This predetermined period is set longer than the time constant of the field winding 5. The inverter 68 inverts the output signal of the timer circuit 67. The AND gate 69 produces a logical product of the output of the first comparator 65 and the output of the inverter 68. The pulse generator 70 generates a clock pulse of low duty ratio. The OR gate 71 produces a logical sum of the

output of the AND gate 69 and the output of the pulse generator 70. The power transistor 61 is turned on and off with the output signal of the OR gate 71.

Next, operations of the voltage regulator 6 of this embodiment will be explained.

When the output voltage of the full-wave rectifier 4 is in the range not exceeding Vreg+$\alpha$, namely when no failure occurs in the power supply line 8, the output of the inverter 68 becomes high level and therefore the power transistor 61 is driven in the ordinary voltage control operation.

When a certain failure occurs in the power supply line 8, for example, when a contact failure occurs at the connecting point, a sharp high voltage surge is generated frequently. In this case, if this high voltage surge is not absorbed with the filter 64 and is then inputted to the second comparator 66, the second comparator 66 starts the timer circuit 67. During operation of this timer circuit 67, it is preset to output the high level signal. Therefore, since output of the AND gate 69 is maintained in the low level during this period and the signal of the pulse generator 70 of low duty ratio becomes valid as a drive signal for the power transistor 61, the power transistor 61 is driven with the output signal of this pulse generator 70 to control the supply of the field current. This low duty ratio is preferably from several percent to tens of percent.

The field current flowing into the field winding 5 is rapidly attenuated because magnetic energy thereof is converted to thermal energy with a resistance of the field winding 5 through